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References : Japan Laid-Open Sho 52-52582
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[Title of the Invention]

Method of manufacturing a MOS transistor

[Claim]

1. A method of manufacturing a MOS transistor comprising:

a step of forming a first insulating film by thermal oxidation of a first major surface of a semiconductor substrate having a first and a second main surface,

a step of forming a first gate electrode on said first insulating film,

a step of forming a support body by putting a insulating layer on said first gate electrode and said first insulating film,

a step of making a side of said second main surface of said semiconductor substrate a thin film to form a third main surface,

a step of forming a second insulating film by thermal oxidation of said third main surface, and

a step of forming a second gate electrode on said second insulating film.

[Detailed Explanation of the Invention]

[Field of Industrial Application]

The present invention relates to a method of manufacturing a MOS transistor having a pair of gate electrodes with a semiconductor layer between them.

[Summary of the Invention]

The present invention makes interfacial characteristic of a gate insulating film and a semiconductor layer better and improves controllability of thickness of a gate insulating film, and makes planarization of a structure possible,

by a method of manufacturing a MOS transistor comprising; a step of forming a first insulating film by thermal oxidation of a first major surface of a semiconductor substrate, a step of forming a first gate electrode on said first insulating film, a step of forming a support body over said first gate electrode and said first insulating film with an insulating layer therebetween, a step of making said semiconductor substrate a thin film to form a second main surface, a step of forming a second insulating film by thermal oxidation of said second main surface, and a step of forming a second gate electrode on said second insulating film.

[Prior Art]

A prior method of manufacturing a MOS transistor is explained based on a cross section of a prior a MOS transistor shown Figure 9.

First, a first gate electrode 2 is formed by patterning after depositing poly-Si on a quartz substrate 1. Then a gate insulating film 3 is formed by depositing on an exposed surface of a quartz substrate 1 and a first gate electrode 2 by a CVD method. And a fixed active layer 4 is formed after depositing Poly-Si on the gate insulating film 3 by a CVD method. Then

after a gate insulating film 5 made of SiO_2 is deposited by a CVD method, a second gate electrode 6 is made of Poly-Si above the active layer 4 with this gate insulating film 5 between them. Then, a source region A and a drain region4B are formed by ion implanting an impurity for source and drain in a self-alignment manner with respect to the gate electrode. Further, it is almost manufactured by forming an insulating film 7 and a contact electrode 8, 8.

[Problem To Be Solved By The Invention]

However, there is a problem in such a prior art that the interfacial characteristics is not good because each of the active layer 4, gate insulating layers 3 and 5, and the first and second gate electrode 2 and 6 is formed in each step respectively.

The present invention is to solve the above-described problems and has an object to provide a method of manufacturing a MOS transistor as a compact, so called SOI element, in which an interfacial characteristic of the semiconductor layer and the insulating layer is good.

[Means To Solve The Problems]

In order to achieve the above-described objects, the method of manufacturing a MOS transistor comprising; a step of forming a first insulating film by thermal oxidation of a first major surface of a semiconductor substrate having a first and a second main surfaces, a step of forming a first gate electrode on said first insulating film, a step of forming a support body over said first gate electrode and said first insulating film with an insulating film therebetween, a step of making a side of said second main surface of said semiconductor substrate a thin film to form a third main surface, a step of forming a second insulating film by thermal oxidation of said third main surface, and a step of forming a second gate electrode on said second insulating film.

[Action]

By forming first and second insulating films on the first and third main surfaces of the semiconductor substrate by

thermal oxidation makes an interfacial characteristic of the semiconductor layer and the insulating films better and improves controllability of the element.

[Example]

A detail of the method of manufacturing a MOS transistor related with the present invention is explained based on examples shown in the figures as follows.

In the figure, 11 is a semiconductor substrate made of silicon and a first gate insulating film 12 is formed by thermal oxidation of a side of said semiconductor substrate 11 in an oxidation atmosphere at a high temperature (Figure 1). Then a poly-Si layer 3 to be a gate electrode is laminated (Figure 2) and a first gate electrode 3A is formed by making a window through lithography (Figure 3). Further, an insulating layer 14 is formed by growing SiO_2 by a CVD method (Figure 4), a support body is formed by growing poly-Si thick on said insulating layer by a CVD method.

Then, as shown in Figure 6, said support body 15 is fixed, and said semiconductor substrate 11 is ground to form a thin film. Then a surface of the semiconductor substrate 11 is oxidized by heat in an oxidation atmosphere at a high temperature to form a second gate insulating film 16 in the same way as above-described gate insulating film 12 (Figure7), and then a second gate electrode 17 is made of poly-Si. Furthermore, a protective film 18 made of SiO_2 is formed on a predetermined point. Then as shown in Figure 8, a contact electrode 19 is made of aluminum, with the result that a MOS transistor is completed.

Further, in this example, the gate length of the second gate electrode 17 is set shorter than the first gate electrode 13A. When diffusing an impurity for source and drain, the impurity is diffused in a self-alignment with respect to the first gate electrode 13A as a mask, and is diffused in a self-alignment with respect to the second gate electrode 17 as a mask. Thus, a profile is made in the doping concentration of the source region 11A and the drain region 11B and hence a

known LDD structure is formed.

Also, the thickness of the semiconductor substrate 11 to be a channel region in the present example is a thin film not more than about 100nm by the above-described grinding step, and a mobility μ is set up at large.

As described the present example above, furthermore, it is possible to change every design. For example, in the case of the above present example, the source region 11A and drain region 11B are formed by self-align by using the first gate electrode 13A and the second gate electrode 17, but it is certainly possible to form by self-align by using only one of the gate electrodes.

Also, regarding the above example, the thickness of the semiconductor substrate 11 to be a channel region is not more than about 100nm, but it is not limited to this.

Furthermore, regarding the above examples, a support body 15 is grown by a CVD method, but it is certainly possible to use a method of bonding a support body.

[Effect of the Invention]

As is clear from the above mentioned explanation, a method of a MOS transistor of the present invention has effects; it makes an interfacial characteristic of a semiconductor layer to be a channel region and a gate insulating film better and improves controllability of thickness of a film(s), and it makes planarization of structure possible and makes it more compact.

[Brief Explanation of Drawings]

Fig. 1~8 are cross sections which show each process of a method of manufacturing a MOS transistor of the present invention, Fig. 9 is a cross section which shows a prior example.

[Explanation of Marks]

11---a semiconductor substrate

12---a first gate insulating film

13A---a first gate electrode

16---a second gate insulating film

17---a second gate electrode